

What is claimed is:

1. A method for fabricating an image sensor including a device isolation layer having a trench structure, wherein an  
5 image sensor is integrated with a depletion mode transistor and a typical transistor, the method comprising the steps of:

forming sequentially a buffer oxide layer and a pad nitride layer on a substrate;

10 patterning the pad nitride layer and the buffer oxide layer formed on a first region for the depletion mode transistor and a second region for the typical transistor by performing a device isolation mask process and an etch process to form trenches in the first region and the second region;

forming a spacer at lateral sides of the trenches;

15 masking the second region to form a high concentration of a first channel stop ion implantation region at a bottom side of the transistor in the first region by using high energy;

removing the spacer formed at the lateral sides of the trench in the first and the second regions;

20 masking the second region to form a low concentration of a second channel stop ion implantation region with use of low energy so that the second channel stop ion implantation region encompasses the lateral sides and the bottom side of the trench in the first region; and

25 burying an insulation material into the trenches in the first region and the second region.

2. The method as recited in claim 1, wherein the first channel stop ion implantation region is formed by employing high energy of about 150 KeV to about 250 KeV and a concentration ranging from about  $6.0 \times 10^{12} \text{ cm}^{-3}$  to about  $1.5 \times 10^{13} \text{ cm}^{-3}$ .

3. The method as recited in claim 1, wherein the ion implantation process for forming the second channel stop ion implantation region is performed by giving a tilt angle and a rotation.

4. The method as recited in claim 3, wherein the second channel stop ion implantation region is formed by employing low energy of about 40 KeV and a concentration of about about  $6.0 \times 10^{12} \text{ cm}^{-3}$ .

5. The method as recited in claim 2, wherein the first and the second channel stop ion implantation regions are formed by using boron B<sub>11</sub>.

6. The method as recited in claim 1, wherein the spacer is a tetra-ethyl-ortho-silicate (TEOS) oxide layer.